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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,244	09/29/2003	Christian Muller	59992 (45107)	3489

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,244	MULLER ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication app ars on the cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-29-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: the disclosure: "the load section of the MOSFET P4 and the resistor R1", "the load section of the two transistors P4 and P6", the load section of transistor P3 in the last paragraph of page 13, are ambiguous because it is not clear what is the **load section** of the MOSFET P4 and the **load sections** of the two transistors P4 and P6. The applicant is requested to explain clearly what is "the load section" of a transistor. The same analysis is true for other "load section" or "load sections" in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and or clarification is required.

Regarding claim 1, the recitation "at least two first transistors, the **load sections** of which are **switched in series** and connect the circuit node **with a voltage**" on lines 3-5 is indefinite because it is not clear what are the load section of the transistors and " **a voltage**". This recitation is also misdescriptive. In figure 1 of the present application, assumed that the two first transistors are (P1) and (P2) then these two transistors are **directly** connected in cascode. They are not **"switched in series"** because there is no switching device between

them to perform the switch connection. The same analysis is true for the recitations "at least two second transistors, the **load sections** of which **are switched in series** and connect the circuit node with a reference potential" on lines 6-8 and "the load section" in claim 8. The applicant is requested to define what is the **load section** of a transistor.

Claim 4 is indefinite because it is not clear what are the "a pre-set voltage in the inactive state" and the "at least one threshold value". It is not clear how the circuit can detect when the voltage on the circuit node (10) exceeds the " **threshold value**".

Regarding claim 8, the recitation "the control circuit comprises an electrical path, which comprises the **load section of a transistor** controlled by the **enabling signal**" on lines 2-4 is indefinite because it is misdescriptive. Assumed that the "a transistor" is transistor (P3) of figure 1, the **gate** of transistor (P3) is coupled to the enabling signal (ENQ). No "**load section**" of transistor (P3) is seen controlled by the enabling signal (ENQ). The recitation "connected on the one hand with a further voltage and on the other hand with a diode and serves to **regulate the control voltages** in **the inactive state**, as long as the voltage on the circuit node is below the at least **one threshold value**" is indefinite because it is misdescriptive. Figure 1 shows that when in the inactive state, transistor (P2) is turned off. Thus, diode (D1) is not served to regulate the control voltage (Up2) as recited. It is also not clear what the "at least one threshold value" is meant by. Explanation is required.

Regarding claim 9, the recitation "in the active state it consumes no static power" is indefinite because it is misdescriptive. Figure 1 shows that in the active state, signal (ENQ) is low, transistor (P5) is constantly turned on and a static current flows from terminal (U10) to the ground.

Claims 2, 3, 5-7, and 10-13 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, and 10-13 are rejected under 35, U.S.C. 102(b) as being anticipated by Hung et al. (6,018,257).

Regarding claim 1, figure 9 of Hung shows a diver circuit with circuit node (OUTPUT);

at least two first transistors (102, 202 connected in cascode) connect the circuit node with a voltage (3.3V);

at least two second transistors (104, 204) connected cascode) connect the circuit node with a reference potential (GND), and

a control circuit (502, 504, 302, 515, 506, 508, 510, 602, 502', 504', 506', 508' 510' and 512'), which is designed in order to regulate at least a first control voltage (210) on at least one transistor of the at least two first transistors and at least a second control voltage (214) on at least one transistor of the at least two second transistors dependent on a voltage at the circuit node (OUTPUT).

Regarding claim 2, when the enabling signal (INPUT, INPUT/) is activated/deactivated, the driver is in the active or an inactive state.

Regarding claim 3, control circuit is also designed in order to regulate the control voltages in the active state in such a manner that the transistors (204, 202) controlled by the control voltages are approximately in saturation (col.4, lines 27-30).

Regarding claim 4, when the output voltage goes up to 5.5V, the control voltage at node (214) is **reduced** to 3.6V and the gate-source voltage (Vgs) of transistor (204) is reduced to 1.9V (col. 5, lines 23-31).

Regarding claim 5, the electrical path is (512', 506' and diode 510').

Regarding claims 10-12, all the transistors of figure 9 are MOSFETs and the two first transistors (102, 202) are P channel MOSFETs and the two second transistors (104, 204) are n-channel MOSFETs.

Regarding claim 13, the well of transistor (102) is biased by 5V.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
05-24-04

TUAN T. LAM
PRIMARY EXAMINER